Remarks

The Office Action mailed September 19, 2005, and made final, has been carefully reviewed and the foregoing amendment has been made in consequence thereof.

Claims 1-19 are now pending in this application. Claims 1-19 stand rejected.

In accordance with 37 C.F.R. 1.136(a), a one month extension of time is submitted herewith to extend the due date of the response to the Office Action dated September 19, 2005, for the above-identified patent application from December 19, 2005, through and including January 19, 2006. In accordance with 37 C.F.R. 1.17(a)(3), authorization to charge a deposit account in the amount of $120.00 to cover this extension of time request also is submitted herewith.

The rejection of Claims 1-5 and 7-12 under 35 U.S.C. § 103 as being unpatentable over Robinson (U.S. Patent 5,708,838) in view of Robinson (U.S. Patent 6,567,837) is respectfully traversed.

Robinson '838 describes a system 100 which includes a host processor 102, and a plurality of object oriented processors 104, 106, 108 which are coupled to host processor 102 via a Comms bus 110. Each of the object oriented processors 104, 106, 108 includes a Comms interface 104a, 106a, 108a, an intelligent message handler 104b, 106b, 108b, and a hardware (peripheral) interface 104c, 106c, 108c. Each object oriented processor 104, 106, 108 is bi-directionally coupled via its respective Comms interface 104a, 106a, 108a to the Comms bus 110 which is coupled to host processor 102. High level messages sent by host processor 102, as instructed by the host software 103, are interpreted by the respective intelligent message handlers 104b, 106b, 108b and used to control the respective hardware interfaces 104c, 106c, 108c to control peripheral devices. Similarly, data from the peripheral devices are received by the respective hardware interfaces 104c, 106c, 108c, interpreted by the respective intelligent

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message handlers 104b, 106b, 108b and transmitted to the host as high level messages. Column 7, lines 35-60.

However, and as indicated in the Office Action at page 5, Robinson '838 does not teach that the class processors have an associated protected localized read/write memory that is accessible to itself and other class processors of the same class.

Referring to Robinson '837, it describes that an instantiation layer of the object calls a memory manager 38 and requests an allocation of RAM 14. The memory manager checks for the availability of RAM at 220 and if enough RAM is available, the memory manager 38 returns a pointer to a starting address in RAM to the instantiation layer which receives the pointer and arranges its memory at 224. Column 10, lines 10-22. At Column 10, lines 30-38, Robinson '837 indicates that "[w]hen an object is instantiated, the instantiation layer arranges (at 224) its allocated RAM into organized parts. The first part is the output message header which includes a pointer to the output buffer of the object instantiation, the message length, the active task list index, the flow priority of the object instantiation, the message type, and the source ID. This first part is common to all objects, i.e. all instantiated objects arrange part of their allocated RAM in this manner. One or more other parts of RAM are arranged for private data used by the instantiated object in the performance of its functionality." However, Robinson '837 does not describe, nor suggest, class processors having each of an associated private localized read/write memory, an associated protected localized read/write memory, and a public localized read/write memory.

Claim 1 recites a distributed processing system that comprises "a host processor including a host communication infrastructure (HCI) configured to provide communication with said host processor," " a plurality of class processors each comprising an associated private localized read/write memory, an associated protected localized read/write memory, and public localized read/write memory " and "a plurality of application program interface modules" ... "each defining a programming interface for a respective said class processor...".

Robinson '838 in view of Robinson '837 do not describe nor suggest such a system. Specifically, Neither Robinson '838, nor Robinson '837 describe or suggest class processors each comprising an associated private localized read/write memory, an associated protected localized read/write memory, and public localized read/write memory. Rather, Robinson '837 only recites that one or more other parts of RAM are arranged for private data used by the instantiated object in the performance of its functionality which is not suggestive of the recited private memory, protected memory, and public memory.

The Office Action in paragraph 5, page 3, for example, purports that the claim element of an "associated protected localized read/write memory" is described by Robinson '837 by combining the recitations of Column 10, lines 30-35 and Column 17, line 63 to Column 18, line 2. Applicants respectfully disagree. The recitations of Column 10, lines 30-35 describe the first portion of the RAM that has been allocated to an instantiated object. This first portion is described as being an output message header. The memory allocation for this part of the RAM appears to be fixed, at least for as long as the instantiated object exists since at lines 35-38 Robinson '837 states that one or more other parts of RAM are arranged for private data used by the instantiated object in the performance of its functionality.

As such, it is respectfully suggested that the "output message header" for an instantiated object of Robinson '837 is not fairly characterized as an "associated protected localized read/write memory". Since a recitation of a "read/write memory" necessarily implies that the memory may be accessed or updated during operation of the class processor, a header identifying parameters of an instantiated object, presumably fixed for as long as the instantiated object is resident in the allocated RAM, is not illustrative of any type of read/write memory associated with a class processor.

With respect to the Claim 1 recitation of a "public localized read/write memory", Applicants respectfully suggest that Robinson '837 makes no such suggestion. Again referring to the Office Action at page 3, paragraph 5, the Examiner again points to the passage of

Robinson '837 (e.g., Column 10, lines 30-35) that has presumably just described the recitation of Claim 1 directed to an "associated protected localized read/write memory" and suggests that it also suggests the recitation of Claim 1 directed to a "public localized read/write memory".

As previously stated, the recitations of Column 10, lines 30-35 describe the first portion of the RAM that has been allocated to an instantiated object. This first portion is described as being an output message header. The memory allocation for this part of the RAM appears to be fixed, at least for as long as the instantiated object exists since at lines 35-38 Robinson '837 states that one or more other parts of RAM are arranged for private data used by the instantiated object in the performance of its functionality.

As above, it is respectfully suggested that the "output message header" for an instantiated object of Robinson '837 is not fairly characterized as a "public localized read/write memory". Since a recitation of a "read/write memory" necessarily implies that the memory may be accessed or updated during operation of the class processor, a header identifying parameters of an instantiated object, presumably fixed for as long as the instantiated object is resident in the allocated RAM, is not illustrative of any type of read/write memory associated with a class processor.

Further, Robinson '837 describes a memory management scheme for a block of contiguous memory, specifically RAM 14, and not class processors each having the associated localized read/write memories as illustrated in Figure 1 of the present application. For all of the reasons set forth above, Claim 1 is submitted to be patentable over Robinson '838 in view of Robinson '837.

Claims 2-5 and 7-12 depend, directly or indirectly, from independent Claim 1 which is submitted as being patentable for the reasons given above. When the recitations of Claims 2-5 and 7-12 are considered in combination with the recitations of Claim 1, Applicants submit that

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dependent Claims 2-5 and 7-12 likewise are patentable over Robinson '838 in view of Robinson '837.

With respect to Claim 5, for example, Robinson '838 in view of Robinson '837 do not describe, nor suggest, an associated protected localized read/write memory accessible only to its class processor and class processors of the same class. Rather, and as described above, Robinson '837 describes an output message header that appears to describe the parameters of an instantiated object and one or more parts of RAM are arranged for private data used by the instantiated object. More specifically, Robinson '837 does not suggest that this private data area of RAM is accessible by other class processors (or other instantiated objects) of the same class as is the case with the associated protected localized read/write memory of Claims 1 and 5.

In addition, Robinson '838 in view of Robinson '837 do not describe nor suggest class processors which include public localized read write memory that is accessible by the host processor as recited, for example, in Claim 10. For these reasons, in addition to those given above, Applicants submit that dependent Claims 2-5- and 7-12 likewise are patentable over Robinson '838 in view of Robinson '837 and further in view of admitted prior art.

The rejection of Claim 6 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Robinson '837 further in view of Kneib (U.S. Patent No. 4,461,238) is respectfully traversed.

Robinson '838 and Robinson '837 are described above. Kneib describes that each dynamically programmable processing element (DPPE) 10 to 13 has an associated input/output data bus as 14 to 17 which is coupled to a common data bus 18 designated as the DSP bus or the digital signal processing bus. Each DPPE functions as a slave processor and can communicate one with the other through a common bidirectional serial bus 20. The serial bus 20 functions to allow the DPPE devices to communicate while the DSP bus 18 allows for the transfer of data between the DPPE devices and a master processor or microprocessor 21. However, neither

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Robinson '837 as described above, nor Kneib describe or suggest, that class processors each
include, private read/write memory, protected read/write memory, and public read/write
memory.

Claim 6 depends from Claim 1 which recites a distributed processing system that
comprises "a host processor including a host communication infrastructure (HCI) configured to
provide communication with said host processor," " a plurality of class processors each
comprising an associated private localized read/write memory, an associated protected localized
read/write memory, and public localized read/write memory " and "a plurality of application
program interface modules" ... "each defining a programming interface for a respective said
class processor...".

Robinson '838 in view of Robinson '837 and further in view of Kneib do not describe nor
suggest such a system. Specifically, None of Robinson '838, Robinson '837, and Kneib describe
or suggest class processors each comprising an associated private localized read/write memory,
an associated protected localized read/write memory, and public localized read/write memory.
For the reasons set forth above, Claim 1 is submitted to be patentable over Robinson '838 in
view of Robinson '837 and further in view of Kneib.

Claim 6 depends from independent Claim 1 which is submitted as being patentable for
the reasons given above. When the recitations of Claim 6 are considered in combination with the
recitations of Claim 1, Applicants submit that dependent Claim 6 likewise is patentable over
Robinson '838 in view of Robinson '837 and further in view of Kneib.

The rejection of Claim 13 under 35 U.S.C. § 103 as being unpatentable over Robinson
'838 in view of Patel et al. (U.S. Patent No. 5,513,369) is respectfully traversed.

Robinson '838 is described above. Patel et al. describe subsystems each including a
plurality of processors 14, each of which is linked to a star coupler device 20 by a cable 12.

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Cables 18 interconnect the star coupler devices of each subsystem.   Each star coupler device 20
includes two star couplers 22 and 24. Star coupler 22 is connected via cables 12 with processors
14. Each cable includes a pair of conductors, one of which is connected to carry messages from
the associated processor to the star coupler, while the second conductor conducts messages from
the star coupler device to its associated processor. Within each subsystem, star coupler 22
operates in a conventional manner such that any message that is received by star coupler 22 from
a linked processor 14 via cables 12 will be retransmitted to each of the linked processors,
including the processor that generated the message.

Claim 13 recites a method for designing a distributed processing system for an
application. The method comprises the steps of "configuring a plurality of class processors to
compute the functions into which the application is partitioned in response to the data messages"
and " configuring each class processor with an associated private localized read/write memory,
an associated protected localized read/write memory, and public localized read/write memory".

Robinson '838 in view of Patel et al. do not describe, nor suggest the claimed method.
Specifically, Robinson '838 in view of Patel et al. do not describe nor suggest configuring each
of a plurality of class processors with an associated private localized read/write memory, an
associated protected localized read/write memory, and public localized read/write memory.
Referring to the Office Action starting at page 8, paragraphs 19-22, it is apparent that the
Examiner has not taken into consideration the amendments to Claim 13 entered in the July 5,
2005 Amendment. Robinson '838 describes pre-partitioned object oriented processors which are
configured to respond to specifically addressed messages from the host processor. Patel et al.
describe a system where each processor is directly connected to a host processor which manages
and distributes the processing load amongst the other processors. Defining private, protected,
and public read/write memories for each individual class processor is not described nor
suggested.

For the reasons set forth above, Claim 13 is submitted to be patentable over Robinson '838 in view of Patel et al.

The rejection of Claims 14 and 17-18 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Patel et al. and further in view of Robinson '837 is respectfully traversed.

Claims 14 and 17-18 depend, directly or indirectly, from independent Claim 13 which is submitted as being patentable for the reasons given above. When the recitations of Claims 14 and 17-18 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 14 and 17-18 likewise are patentable over Robinson '838 in view of Patel et al. and further in view of Robinson '837.

Further, Robinson '838 in view of Patel et al. and further in view of Robinson '837 do not describe nor suggest a class processor having an associated private localized read/write memory, an associated protected localized read/write memory, and public localized read/write memory. Rather, a memory management scheme for a block of contiguous memory is described, specifically, Robinson '837 describes where one or more parts of RAM are arranged for private data by an instantiated object. As described extensively above, Robinson '837 does not describe nor suggest either an associated protected localized read/write memory or a public localized read/write memory. In addition, Robinson '837 does not suggest that this private data area of RAM is accessible by other class processors (or other instantiated objects) of the same class.

For these reasons, in addition to those given above, Applicants submit that dependent Claims 14, 17, and 18 are patentable over Robinson '838 in view of Patel et al. and further in view of Robinson '837.

The rejection of Claims 15 and 16 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Robinson '837 and Patel et al. and further in view of admitted prior art is respectfully traversed.

Claims 15 and 16 depend, directly or indirectly, from independent Claim 13 which is submitted as being patentable for the reasons given above. When the recitations of Claims 15 and 16 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 15 and 16 likewise are patentable over Robinson '838 in view of Robinson '837 and Patel et al. and further in view of admitted prior art. Further, Robinson '838 in view of Robinson '837 and Patel et al. and further in view of admitted prior art do not describe nor suggest class processors comprising a protected read/write memory as recited in Claim 16.

The rejection of Claim 19 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Patel et al. and further in view of admitted prior art is respectfully traversed.

Claim 19 depends from independent Claim 13 which is submitted as being patentable for the reasons given above. When the recitations of Claim 19 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claim 19 likewise is patentable over Robinson '838 in view of Patel et al. and further in view of admitted prior art.

In addition to all of the reasons given above, Applicants respectfully submit that the Section 103 rejections of the presently pending claims are not proper rejections. As is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Robinson '838, Robinson '837, Patel et al., Kneib or the admitted prior art, considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertions within the Office Action, Applicants respectfully submit that it would not be obvious to one skilled in the art to variously combine Robinson '838, Robinson '837, Patel et al., Kneib, and the admitted prior art, because there is no motivation to combine the

references suggested in the art. Additionally, the Examiner has not pointed to any prior art that teaches or suggests to combine the disclosures, other than Applicants' own teaching. Rather, only conclusory statements like "it would have been obvious to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array that utilizes memory in an efficient manner" suggests combining the disclosures.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicants' disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck , 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejections are based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, Robinson '838 is cited for its teaching of a host processor communicating with object oriented processors, albeit not through application program interface modules each define a programming interface. Robinson '837 is cited for its teaching of memory management of contiguous memory, Kneib is cited for teaching a secondary bus through which dynamically programmable processing elements communicate, Patel et al. is cited for teaching

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star processing configurations, and the admitted prior art is cited merely for teaching single chip integrated circuit fabrication. Since there is no teaching nor suggestion in the cited art for the various combinations, the Section 103 rejections appear to be based on hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicants request that the Section 103 rejections of Claims 1-19 be withdrawn.

In addition, as is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Robinson '838, Robinson '837, Kneib, Patel et al. and the admitted prior art, considered alone or in combination, describe or suggest the distributed processing system and associated methods as recited in the claims. Further, these references do not provide any motivation for their various combinations as suggested by the Office Action. For these reasons, in addition to the reasons set forth above, Applicants request that the Section 103 rejections of Claims 1-19 be withdrawn.

In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,

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